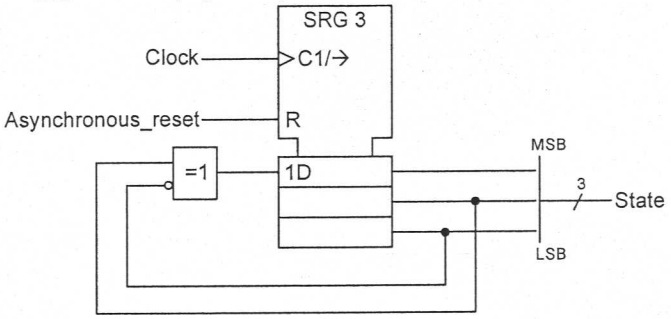
## PROBLEM 1.

**a)** Logic architecture of a finite state machine is shown in Figure below. Draw the state diagram of the state machine assuming that the initial state is "000". (3 points)

**b)** What is the highest possible clock frequency tolerated by the state machine? Assume the delay of the XOR gate is $t_{xor}$ = 1 ns and the delay of the shift register from clock input to data output is $t_{srg}$ = 3 ns. For the sift register's data input the setup time is $t_{setup}$ = 1ns and the hold time is $t_{hold}$ = 1 ns. (2 points)

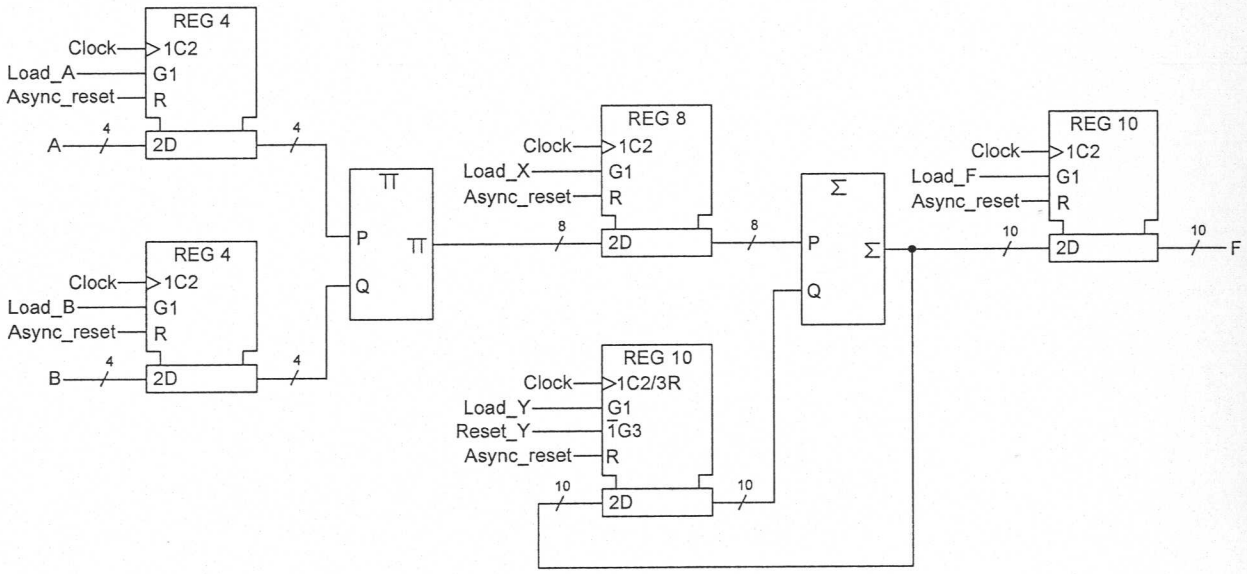



**State machine for the problem 1.**

## PROBLEM 2.

**a)** You have to place into a design a register that can store values between [-5.25, 5.25] in binary format. How many bits at least the register should be wide and where should the binary point be if the accuracy of 0.0625 is demanded for the values to be stored? (1 point)

**b)** Design such control logic for the data path architecture shown in Figure below that the data path calculates algorithm F = 3 x (A x B). The calculation should begin when the user gives one clock period long "start" signal. Assume that the variable A and B are readable during the clock period following the "start" signal. Draw the state diagram (2 points) and the logic architecture (2 points) of the control logic to be designed.




**Data path for the problem 2.**

## PROBLEM 3.

a) Draw a logic-architecture composed of adders so that it multiplies 6-bit positive integer (A) by a base-10 **constant** $26_{10}$. The result must be a normal arithmetic product (e.g., if the multiplicand is 20, so the product is $26_{10} \times 20_{10} = 520_{10}$). Only adder circuits are allowed in the architecture diagram. Draw a bit accurate architecture using the symbols found in the dependency notation standard (IEEE std 91a-1991 = SFS 4612). The internal logic structure of adders is not needed to be shown. (3 points)

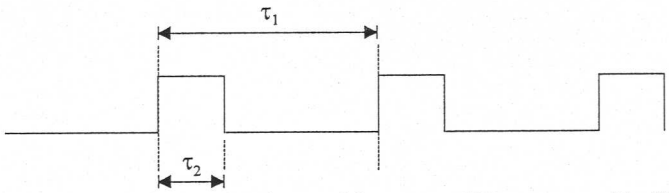
b) Write logic states (1 or 0) of all the signal nodes in the architecture you draw in the previous part a) of this problem, in the case, the multiplicand is $33_{10}$. (2 points)

## PROBLEM 4.

In Fig.4, you can see a Register Transfer Level (RTL) architecture. The output frequency of the oscillator is $2^{15}$ Hz = 32 768 Hz.

a) Architecture in Fig. 4 implements a clock logic which is capable to count and show seconds, minutes and hours of a day. How you can set the clock to show the right time? (1 point)

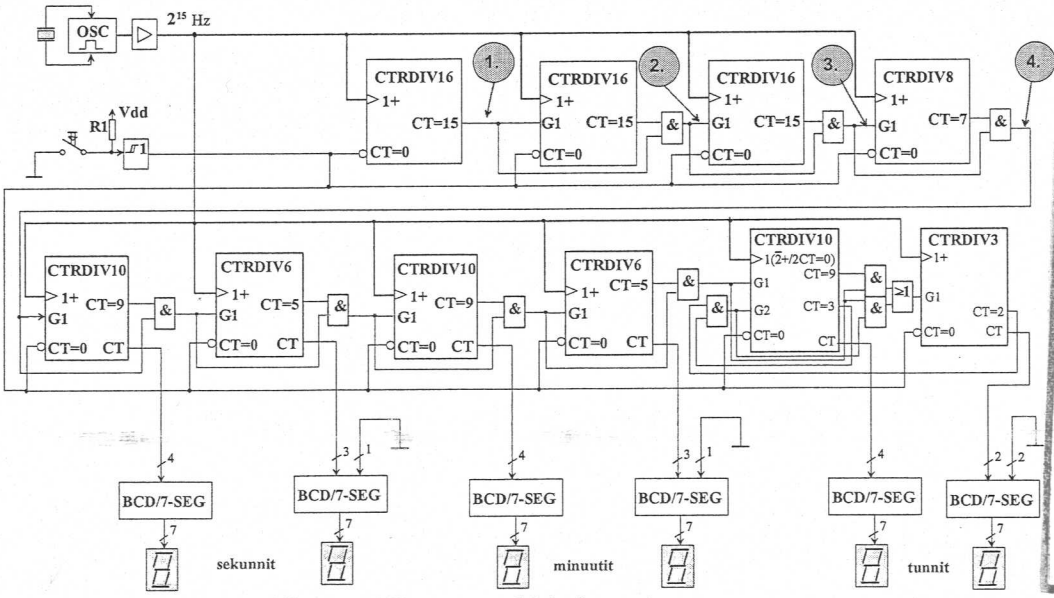
b) The signal waveform in nodes 1, 2, 3 and 4 are like in the figure below. Solve the numerical values of parameters $\tau_1$ and $\tau_2$ in signal nodes 1 … 4. (1 point)




c) There are 10 digital counters in the architecture. How many D-flip-flops are needed to implement them altogether. Specify the number of DFFs of every counter type. A pure number is not a sufficient answer. (1 point)

d) How you can use the number of flip-flops to estimate the equivalent gate count of an ASIC implementation of the whole architecture. How you can use the number of flip-flops to estimate the use of FPGA resources (Look-up Tables (LUTs), flip-flops, memory bits, I/O-pins …). (1 point)

e) There are 6 BCD/7SEG decoders in the architecture. How many 4-input Look-Up Tables (LUT-4) are needed to implement them in a FPGA platform? How the estimation is different if there are 6-input Look-Up Tables available in the platform. (1 point)




Kuva 4. Tehtävään 4 liittyvä RT-tason arkkitehtuuri.