1. (5 p.) Consider a digital thermometer. The temperature range to be measured is -32 … +31 °C. The temperature sensor converts this temperature range to voltages 0 V … 6.4 V, where about 0 V corresponds to temperature -32 °C, about 3.2 V corresponds to 0 °C and about 6.4 V corresponds to temperature +31 °C. An analogue-to-digital converter (AD-converter) converts the output voltage of the sensor to unsigned binary number to range 0 … 2^n-1, where n is the number of bits and output word 0 corresponds to temperature -32 °C, $2^n/2$ corresponds to temperature 0 °C and 2^n-1 to temperature +31 °C. To easily distinguish the negative and positive measurement results the output of the AD-converter is converted to two's complement format, in which the digital word with n zeroes corresponds to temperature 0 °C. Because the measurement results are presented with 7-segment display the results must be converted to sign-magnitude format if necessary. With sign-magnitude format the sign bit (left most bit) controls the sign segment of the display, whereas the other bits (magnitude) control the 7-segment displays for the absolute value of the temperature after suitable code conversions.

a) how many bits are needed to present the measurement result of the above mentioned digital thermometer as a digital number with 0.5 °C resolution?

b) how in this case the n-bit unsigned binary number of the AD-converter is converted to two's complement format, in which the digital word with n zeroes corresponds to temperature 0 °C?

c) what must be done with the unsigned binary numbers of the AD-converter representing a positive temperature to see a correct reading in the display?

d) what must be done with the unsigned binary numbers of the AD-converter representing a negative temperature to see a correct reading in the display?

e) what code conversions are needed to show the sign-magnitude format results in the 7-segment display in decimal number system?

2. (5 p.) Fill in the following table representing the signal values of the digital thermometer of assignment 1, when one signal value is given, and the output of the AD-converter has 6 bits, i.e. n = 6. Note the location of the origin!

Temperature [°C]	Sensor voltage [V]	Output of the AD-converter as unsigned binary	6-bit two's complement, when 0 °C -> 0	one's complement	sign-magnitude
9					
	2.3				
		110100			
			101110		
					001111

3. (4 p.) Design a combinational logic that converts the 3-bit two's complement format binary number to 3-bit sign-magnitude format. Mark the inputs with symbols A, B, C and the outputs with V, X, Y. If the absolute value of the binary number ABC exceeds the range of the 3-bit sign-magnitude output the logic does not perform any conversion, i.e. VXY=ABC. Present:

a) thruth table

b) the Karnaugh maps of the outputs V, X and Y

c) the minimised logic functions of the outputs V, X and Y as sums of products

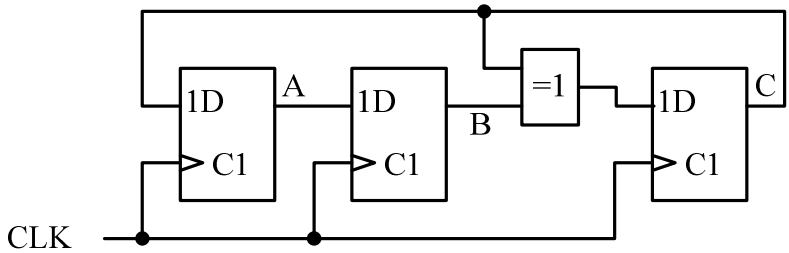
d) the logic diagrams of the outputs V, X and Y using 2- and 3-input AND- and OR-gates and NOT-gates.

4. (3 p.) Analyse the operation of the following synchronous state machine. The initial state is ABC=100.

a) how many allowed states does the state machine have normally?

b) present the operation of the logic over o period of ten clock cycles as a timing diagram or as a table

c) what will happen if the state machine goes into state ABC = 000?



Alkutila (ABC) = 100
Initial state (ABC) = 100

5. (3 p.) Using the following digital blocks realise a frequency counter that measures the frequency f_{in} of the input signal in. The measurement range is 1…9999 Hz. The unit of the output signal out is Hz. The frequency f_{clk} of the clock signal clk clocking all flip-flops is 32768 Hz. The behavior of the design must be synchronous, i.e. except for the power-up-reset (initialisation with signal reset, when the device is powered up), all changes in the flip-flops happen synchronously to the clock signal clk. For example marking CT=0 in the output means that the corresponding output is 1 when the counter is in state 0. With input signal the CT=0 resets (zeroes) the content of the counter/register. In the marking $> 1, \overline{2} + / 2CT = 0$ symbol > means a clock input that reacts to the rising edge of the clock signal, and $1, \overline{2} +$ means, that when the control signal G1 is 1 and G2 is 0 the content of the counter is incremented by one, and the marking $2CT = 0$ means, that when the control signal G2 is 1 the content of the counter (CT = Content) is zeroed synchronously with the next rising edge of the clock signal. The marking >1C2 of a register means that a new value from the data input 2D is loaded to the register with the rising edge of the clock signal if the control signal G1 is a logic one. The marking C1/→ of the shift register SREG3 means that at the rising edge of the clock signal the first register is loaded with the input signal (1D = in) and the other registers are loaded with the value of the previous register, i.e. the bits are shifted is the registers.

a) connect the blocks with wires and buses (several wires together as a logical entity) in such a way that the logic realises the above mentioned frequency counter

b) draw the timing diagram of the output of the AND-gate following the block SREG3 (3-bit shift register) over five clock cycles when f_{in} is much smaller f_{clk} and signal in changes from zero to one during the first clock cycle.

c) define the parameters m,n,p and r. Please explain!