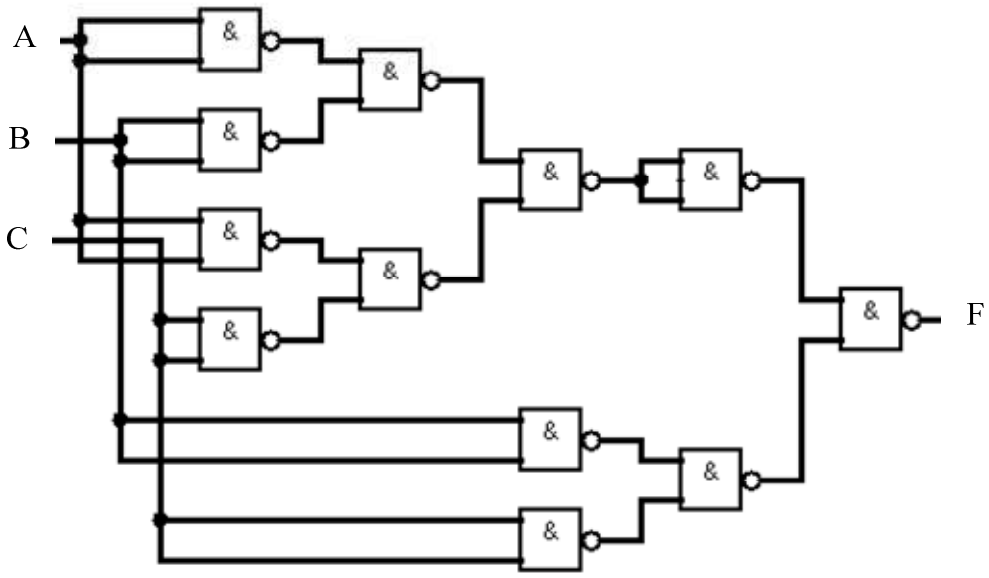
1. a) Present the binary number representing the decimal number -27 as an 8-bit two's complement binary number
b) present the result of 1.a) as a hexadecimal number (base 16)
c) if the 6-bit binary number 100101 is said to represent the number -5 as a decimal number, in which format the binary number 100101 is presented?

2. a) Present the arithmetic multiplication of 3-bit unsigned binary numbers 110 and 110 with pen and paper –method including the result of the multiplication
b) how many bits are needed to present the result of the multiplication of 2.a)?
c) what combinational logic gates and logic blocks are needed to realise the multiplication of 2.a)?

3. To increase the realibility of digital logic with the so called majority logic the value of the output signal depends on the number of zeros and ones in the input signals. If there are more zeros than ones in the input signals the output is zero. If there are more ones than zeros in the input signals the output is one. For the 3-input majority logic (three inputs, e.g. A, B and C, and output F) present:
a) truth table
b) Karnaugh map
c) minimised sum of products for F

4. Analyse the following NAND-logic. Present:
a) truth table
b) Karnaugh map
c) the logic function of F as minimized product of sums



5. Design a synchronous (all flip-flops have a common clock signal) Moore's (outputs coded from the flip-flop outputs) state machine, that can be used for counting tens on hours in a realtime clock, if we want to present the time in format 00:00:00 - 23:59:59. Use D-flip-flops and combinational logic gates. Take into account that this counter must be connected to operate together with the counters counting seconds and minutes as a synchronous digital system, i.e. two control input signals are needed. One control signal G1 is used for enabling the operation of the counter synchronously with the rising edge of the clock signal, and the other control signal G2 forces the counter to synchronously reset with the rising edge of the clock signal. The control signal must be a logic one to activate the corresponding operation. If both G1 and G2 are logic one, the operation of G2 takes action.

a) how many D-flip-flops do you need? Explain!
b) present the state diagram
c) present the state transfer table
d) present the minimised logic functions of the D-flip-flop data inputs as minimized sum of products
e) present the logic diagram

6. a) Complete the following logic diagram with missing wires and
define the parameters b) n, m and c) q and p for the counters CTRnDIVm and CTRqDIVp so, that the output signal once_a_minute of the logic is a logic high for one cycle of the clock signal CLK, and the outputs of the counters can be used for presenting the seconds of a realtime clock. The inputs of the logic are the clock signal CLK (for example 32768 Hz) and a control signal once_a_second, which is a pulse appearing once a second with a width of the cycle of the clock signal CLK. The marking CT means the content of the counter, CTR = counter, DIV = divide (e.g. divides the clock frequency), G1 is enable input and 1+ increments the counter if G1 is a logic one.