Exam: 06.11.2009

Name:_____

Student card number: _____

Assignment 1

Half adder is a digital logic building block that produces the arithmetic sum of two bits (here A and B). The half adder has two outputs, S (sum) and Co (carry out), which together represent the result of the addition. **Present:**

a) the truth table of the half adder

b) the logic diagram of the half adder using the minimum number of 2-input logic gates (AND, OR, NAND, NOR, NOT, XOR, XNOR).

Full adder is a digital logic building block that produces the arithmetic sum of three bits, i.e. the actual bits A and B to be added and the carry in bit Ci. Also the full adder has two output bits, S (sum) and Co (carry out), which together represent the result of the addition. **Present:**

c) the truth table of the full adder

d) the Karnaugh maps for S and Co of the full adder

e) the logic diagram of the full adder using two half adders and one 2-input OR-gate.

Assignment 2

Simulate the operation of the logic below during ten clock cycles in three different cases a)-c). **Draw the timing diagrams.** Assume, that the initial value of the input signal X and the outputs of the D-flip-flops are zero. Signal X is synchronous with the rising edge of the clock signal CLK, i.e. X changes its state just after the rising edge of the clock signal. The first rising edge of X is after the second rising edge of the clock signal.

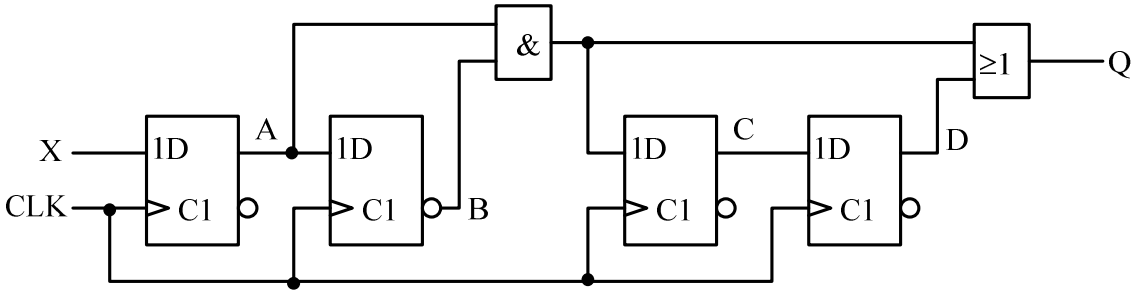
a) X is a pulse with the width of one clock cycle and the distance between the rising edges of X is four clock cycles

b) X is a pulse with the width of one clock cycle and the distance between the rising edges of X is three clock cycles

c) X is a pulse with the width of three clock cycles and the distance between the rising edges of X is four clock cycles

d) what is the logic probably supposed to do if two of the simulations (a-c) produces the correct operation for the output signal Q?

e) what limitations must be set for the timing of the signal X to reach the probably desired operation?



Exam: 06.11.2009

Name:_____

Student card number: _____

Assignment 3

a) Convert a binary number 101111010 to a natural number (positive integer) in decimal system. What is its value as a 2's complement number and in sign-magnitude format?
b) Convert a decimal number 533 to a binary number.
c) How many bits are needed to describe decimal number range 0.0012 … 1.2000?
d) Binary numbers A = 1101001 and B = 00110 are presented in 2's complement format. How much is A + B, A – B and A* B in binary form? Describe each phase of the calculations in binary form (with ones and zeros)? One of the numbers is 8 bit and the other 5 bit long. How this has to be taken in account in different calculations? How do you handle the sign bits in the multiplication?
e) How many Full-Adders are needed to implement the sum A + B of the previous question d)?

Exam: 06.11.2009

Name:_____

Student card number: _____

Assignment 4

R and C of the oscillator in the block diagram below are defined so that its frequency is f hertz (Hz).

a) Draw wave forms in signal nodes 1, 2, 3 4 and 5 in the paper f as a unit.

b) If the frequency in node 1 is 24 kHz, how much is the frequency in nodes 2, 3 4 and 5?

Note that T = (1/f) seconds (s).