Tentti: 07.11.2008

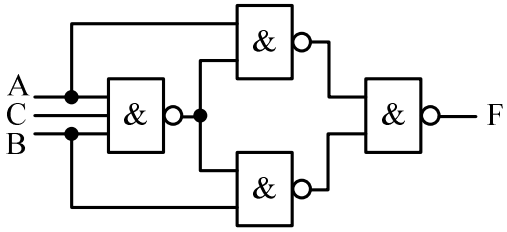
Nimi: _____

Opiskelijakortin numero: _____

Assignment 1

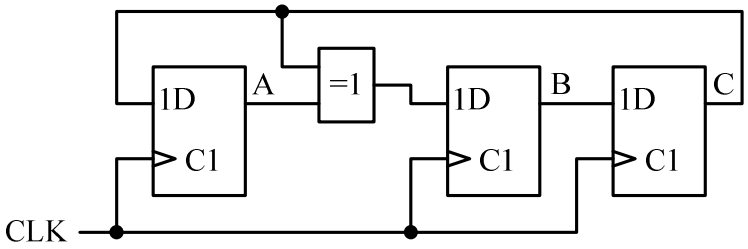
Analyse the operation of the following combinational logic.
a) present the logic function of F as a minimized sum of products
b) present the logic function of F as a minimized product of sums
c) present the Karnaugh map of F
d) if only variables A, B and C are the inputs of the logic, and the complements $\overline{A}, \overline{B}$ *ja* $\overline{C}$ must be done separately with NOT-gates, is the presented logic diagram the most simplified realization for this logic function based on the number of transistor switches? **EXPLAIN!**

- n-input NAND- or NOR-gate = 2n transistors
- n-input AND- or OR-gate = 2n+2 transistors
- NOT-gate = 2 transistors



Assignment 2

a) simulate the following state machine for ten clock cycles. The state machine is initialized to state ABC = 100. Present the simulation result for example as a table, in which the rows represent the clock cycles and the columns are the states of the flip-flops (ABC).
b) how many states does the state machine normally have?
c) what happens if the state machine goes to the state ABC = 000? **EXPLAIN!**
This is a LFSR (Linear Feedback Shift Register).



Alkutila (ABC) = 100
Initial state (ABC) = 100

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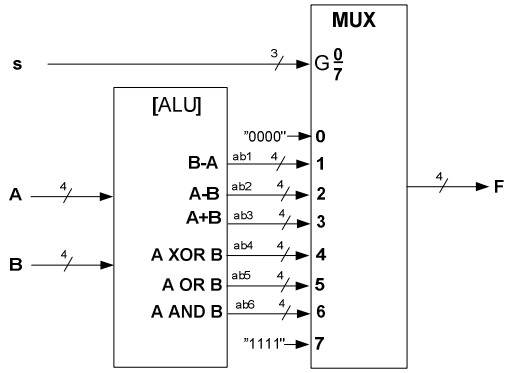
Assignment 3

This assignment deals with the operation of the *Arithmetic Logic Unit = ALU*. The operation of the ALU has been defined with symbols and VHDL-code. Your task is to fill in the simulation table below. Write into the table the values of the signal nodes as hexadecimal numbers. Assume, that numbers A and B are in 2's complement format.

```
Library ieee;
Use ieee.std_logic_1164.ALL;
Use ieee.std_logic_unsigned.All;
ENTITY alu IS
PORT(    s : IN STD_LOGIC_VECTOR(2 DOWNTO 0);
         A,B :IN STD_LOGIC_VECTOR(3 DOWNTO 0);
         F : OUT STD_LOGIC_VECTOR(3 DOWNTO 0));
END alu;

ARCHITECTURE Behavior OF alu is
BEGIN
   PROCESS(s,A,B)
      CASE s IS
         WHEN "000" => F <= "0000";
         WHEN "001" => F <=  B - A;
         WHEN "010" => F <=  A - B;
         WHEN "011" => F <=  A + B;
         WHEN "100" => F <=  A XOR B;
         WHEN "101" => F <=  A  OR B;
         WHEN "110" => F <=  A  AND B;
         WHEN  OTHERS => F <=  A"1111";
      END CASE;
   END PROCESS;
END Behavior;
```



s	0	1	2	3	4	5	6	7
A	1	1	5	3	B	D	A	A
B	F	F	7	2	C	4	C	3

ab1								
ab2								
ab3								
ab4								
ab5								
ab6								
F								

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Assignment 4

This assignment deals with a digital thermometer. The meter converts the measured temperature (point 1.) between -30 °C … +30 °C to a voltage between 0.00 V … 5.00 V (point 2.)

As a result of a measurement the signal level at point 6 corresponds to binary value ’1’. Values at points 4 and 5 corresponds to BCD coded binary vectors”0010” and”1001”, respectively. What digital or analogue signal values have to exist at points 1., 2., 3., 7. and 8 and what can be seen on the display? Binary vector at point 3 could be encoded to a sign-magnitude or 2’s complement form. Give the both options in your answer.