Tentti: 18.05.2007

Nimi: _____

Opiskelijakortin numero: _____

Assignment 1.

Design a logic the output vector S(n:0) of which shows as a binary number the number of ones in the 3-bit input signal A(2:0).
a) What is the value of n in the notation S(n:0)? (1 p)
Present also:
b) the truth table of the logic (1 p)
c) the Karnaugh maps of the bits of the output vector S(n:0) (1 p)
d) the logic functions of the bits of the output vector S(n:0) as minimised sum of products (1 p)
e) the logic functions of the bits of the output vector S(n:0) as minimised product of sums (1 p).

Assignment 2.

Design a synchronous Moore state machine that controls the operation of a simple vending machine. The vending machine releases a candy when coins worth of 50 cents are fed. The coin reader identifies 10 cent and 20 cent coins and notifies the fed coins with logic signals **10cnt** and **20cnt** with a width of one clock cycle. Other coins need not to be considered (they pass the coin reader without a trace). After the reset the state machine is in the initial state **saldo0**. The states of the state machine proceed controlled by the coins fed, that is by the signals **10snt** and **20snt**. When 50 cents of coins is fed the state machine goes to the state **saldo50** in which the output signal **release_candy** is one for one clock period. After the next rising edge of the clock signal the state machine returns to the initial state. If more than 50 cents is fed the output signals **return_coin** and **release_candy** are one for one clock period and after the next rising edge of the clock signal the state machine returns to the initial state. New coins cannot be fed after at least 50 cents is fed but you don't need to worry about that! Keep it simple.
a) How many state variables are needed in a binary coded state machine? **Explain!** (1p)
b) How many state variables are needed in a one hot coded state machine? **Explain!** (1p)
Present also:
c) the state diagram (2 p)
d) the state transfer table. (1 p)

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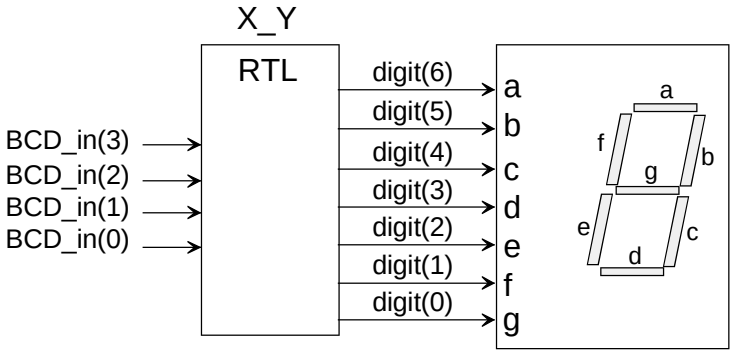
Assignment 3.

The RTL block in the block diagram below behaves as described in the attached VHDL code. What can you see in the 7-segment display if binary vector *BCD_in* gets successively the following hexadecimal (radix-16 numbers) number values A, B, C, D, E and F?




```
 Library ieee;
Use ieee.std_logic_1164.ALL;
Use ieee.std_logic_unsigned.ALL;
--
-- DT1-tentti 18.09.2007
-- © 15.5.2007 Hannu Heusala
--
Entity X_Y is
port (
BCD_in: in bit_vector(3 downto 0);
digit: out bit_vector(6 downto 0)
);
end entity X_Y;
--
architecture RTL of X_Y is
--
type BCD_7SEG_type is array (0 to 15) of bit_vector(6 downto 0);
constant BCD_7SEG: BCD_7SEG_type:=(
--
"1110111","0010010","1011101","1011011","0111010","1101011",
"1101111","1010010","1111111","1111011","1111110","1101101",
"1111001","1011011","0110000","1110111");
--
begin
digit <= BCD_7SEG(conv_integer(BCD_in));
--
end architecture RTL;
```

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Assignment 4.

Microcontrollers (MCU) are known digital integrated circuits (IC). Answer shortly to the following questions concerning the role of microcontrollers in digital electronics.

a) What is a processor core? What digital components (functions) the core of microcontroller includes?

b) What common properties FPGAs and microcontrollers, MCUs, have?

c) How C and VHDL languages are related to microcontrollers?

d) Explain what is the function of data path in a microprocessor core?

e) Explain the functional and structural differences between 3-state and multiplexer-based data path construction in the microcontroller core.