Nimi: _____

Opiskelijakortin numero: _____

PROBLEM 1.

Analyse the combinational logic of figure 1. Present:
a) the logic function of node P_1 as a minimised sum of products
b) the logic function of node P_2 as a minimised product of sums
c) the logic function of node P_3 using a Karnaugh map
d) the logic function of node P_4 with one logic gate
e) the logic function of the output f as a minimised sum of products or otherwise as simply as possible.
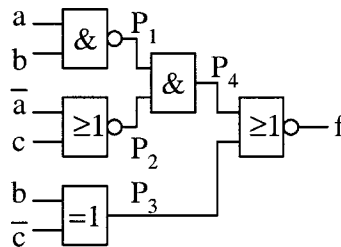Explain your answers adequately!

Figure 1.

PROBLEM 2.

Analyse the operation of the synchronous state machine of figure 2. Present:
a) state diagram
b) state transfer table
c-d) the logic functions of the data inputs of the D-flip-flops as minimised sum of products
e) add to the logic diagram logic gates that can be used for resetting the state machine **synchronously** with the rising edge of the clock signal (Kello) controlled with an input signal SR (synchronous reset). Assume, that the signal SR is synchronous with respect to the clock signal (Kello). Also assume, that the D-flip-flops have an asynchronous reset input connected to a global reset signal (not drawn in the picture).
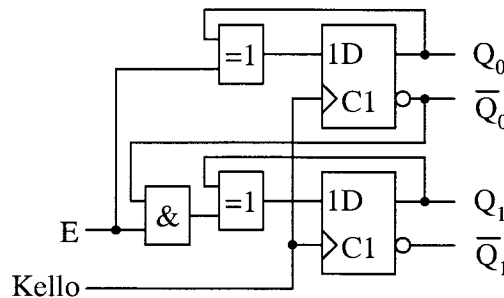

Figure 2.

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PROBLEM 3.

An 8-bit binary number 11001110_2 has been settled on the output pins of an AD-converter. It has been specified that the system understands the number as a positive integer between 0 ... 255.

a) Show the number in the form of a hexadecimal number, i.e., in the base-16 numbering system.

b) Show the number in the form of an octal number, i.e., in the base-8 numbering system.

c) Show the number in the form of a decimal number, i.e., in the base-10 numbering system.

d) Show the number as a binary coded decimal (BCD) number.

e) Show the number as a 7-segment coded display code.

f) Show the number as ASCII coded characters.

TABLE Some number codes

decimal number	BIN 8421	BCD 8421	X-3	DEC 0123456789	7SEG abcdefg	aiken 2421	bikvinääri 5043210	ASCII 6543210
0	0000	0000	0011	1000000000	1111110	0000	0100001	0110000
1	0001	0001	0100	0100000000	0110000	0001	0100010	0110001
2	0010	0010	0101	0010000000	1101101	0010	0100100	0110010
3	0011	0011	0110	0001000000	1111001	0011	0101000	0110011
4	0100	0100	0111	0000100000	0110011	0100	0110000	0110100
5	0101	0101	1000	0000010000	1011011	1011	1000001	0110101
6	0110	0110	1001	0000001000	0011111	1100	1000010	0110110
7	0111	0111	1010	0000000100	1110000	1101	1000100	0110111
8	1000	1000	1011	0000000010	1111111	1110	1001000	0111000
9	1001	1001	1100	0000000001	1110011	1111	1010000	0111001
10	1010	1010	1110	0000000000		0101	000000	
11	1011	1011	1111	0000000011		0110	000001	
12	1100	1100	0000	0000000101		0111	0000010	
13	1101	1101	0001	0000000110		1000	0000011	
14	1110	1110	0010	0000000111		1001	0000101	
15	1111	1111	0011	...		1010	...	
	Unused code words							

O U L U N

YLIOPISTO

Digital Technique I – 521413A
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PROBLEM 4.

The diagram in Fig. 4 describes a data logging logic, which measures temperature values between -50 °C and +50 °C by means of a temperature transducer and converts the analogue output signal by ADC to 10-bit binary words. The binary words are loaded to a RAM. Loading is enabled by the signal *en_load*. The format of the words in the memory is sign/absolute value: sign (0 is "+" and 1 is "-") is the most significant bit and the other 9 bits forms the absolute value of the temperature. The memory address is incremented by the loading of temperature values.

a) How many degrees is the accuracy of temperature values in digital form in the memory?
b) What is the loading frequency? (the frequency of en_load signal?)
c) How long period of time is needed before the memory is full?
d) How many D-FFs are needed to implement counters CTR11 and CTRDIV20k (=CTRDIV20000)?
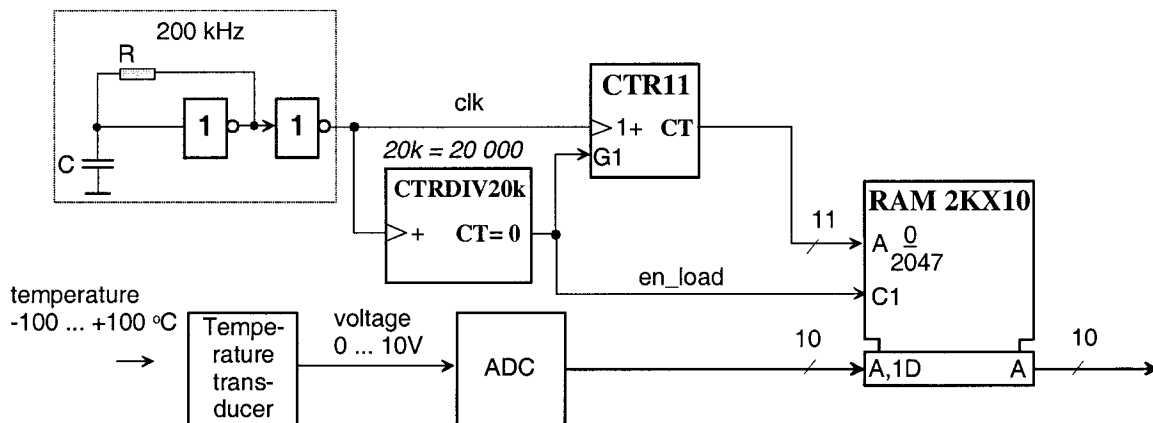e) How fast the ADC must do the conversion?

Fig. 4.