Exam: 03.06.2006

Nimi: ______________________________

Opiskelijakortin numero: ______________________________

PROBLEM 1.

The table below presents the coding of a 7-bit thermometer code (T_7-T_1) to a 3-bit binary code (B_2-B_0) using a highest priority encoder. The first logic one (1) from left in the thermometer code determines the binary number. If we assume, that there are no holes in the thermometer code, as in the table below, the logic function of bit B_0 can be presented as follows.

$$B_0 = T_1\overline{T}_2 + T_3\overline{T}_4 + T_5\overline{T}_6 + T_7$$

$T_7T_6T_5T_4T_3T_2T_1$	$B_2B_1B_0$
0 0 0 0 0 0 0	0 0 0
0 0 0 0 0 0 1	0 0 1
0 0 0 0 0 1 1	0 1 0
0 0 0 0 1 1 1	0 1 1
0 0 0 1 1 1 1	1 0 0
0 0 1 1 1 1 1	1 0 1
0 1 1 1 1 1 1	1 1 0
1 1 1 1 1 1 1	1 1 1

a) using the same assumptions present the logic function of B_1 as minimised sum of products

b) using the same assumptions present the logic function of B_2 as minimised sum of products

c) does the coding of bit B_0 operate correctly if there is a hole in the thermometer code, that is, the code word 0001111 is replaced by 0001101, meaning bit T_2 is inverted? Explain! How do you prevent the effect of this error in the coding of B_0? You can't prevent the hole in the code!

d) does the coding of bit B_0 operate correctly if there is a hole in the thermometer code, that is, the code word 0011111 is replaced by 0010111, meaning bit T_4 is inverted? Explain! How do you prevent the effect of this error in the coding of B_0? You can't prevent the hole in the code!

e) how many different code words are in this thermometer code if all possibilities are concerned, that is, the ones and zeros can be in arbitrary order?

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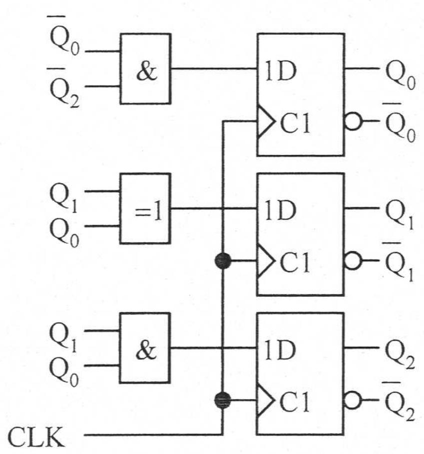
PROBLEM 2.

Analyse the operation of the synchronous state machine presented in the following logic diagram. Let's assume that the flip-flops have been resetted to the state $Q_2Q_1Q_0 = 000$.

a) present the state diagram
b) present the state transfer table
c) are there any unused states in the operating sequence of the state machine? Explain!
d) can the state machine get stuck in an unused state in malfunction without returning to the correct sequence? Explain!
e) modify the logic diagram so that the state machine can be resetted synchronously controlled by a signal synchronous with respect to the clock signal (CLK).



PROBLEM 3.

a) Explain how the acronym FPGA is related to digital technique?

b) Explain how the acronym ASIC is related to digital technique?

c) Explain how the acronym MCU (Microcontroller Unit) is related to digital technique?

d) A 4-input look-up table is a general structure in FPGAs. Explain by examples what kind of logic component it is. In other words, what it can be used for?

e) Explain what it means, if a general qualifying symbol of a graphic symbol for a logic function is **ROM 1024x8**?

OULUN YLIOPISTO

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PROBLEM 4.

The diagram in Fig. 4 describes a data logging logic, which measures temperature values between -100 °C and +100 °C by means of a temperature transducer and converts the analogue output signal by ADC to 12-bit binary words. The binary words are loaded to a RAM. Loading is enabled by the signal *en_load*. The format of the words in the memory is sign/absolute value: sign (0 is "+" and 1 is "-") is the most significant bit and the other 11 bits forms the absolute value of the temperature. The memory address is incremented by the loading of temperature values.

a) How many degrees is the accuracy of temperature values in digital form in the memory?
b) What is the loading frequency? (the frequency of en_load signal?)
c) How long period of time is needed before the memory is full?
d) How many D-FFs are needed to implement counters CTR10 and CTRDIV10k?
e) How fast the ADC must convert?

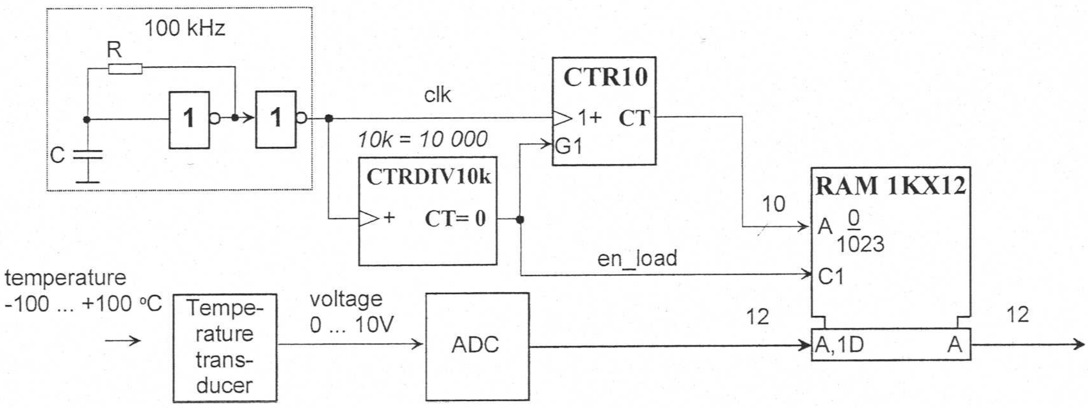

Fig. 4.